THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte HERBERT S. COLE, JAMES W. ROSE, ROBERT J. WOJNAROWSKI and CHARLES W. EICHELBERGER

Appeal No. 93-1883
Application No. 07/759,691[1]

ON BRIEF

Before KIMLIN, GARRIS and PAK, Administrative Patent Judges.

PAK, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the examiner's refusal to allow claims 2 through 6 and 11 through 13, which are all of the claims remaining in the application. Claims 2,

[1] Application for patent filed September 6, 1991. According to the appellants, the application is a continuation of Application No. 07/559,532, filed July 19, 1990, now abandoned, which is a continuation of Application No. 07/305,314, filed February 3, 1989, now abandoned.

4, 11 and 13 have been amended subsequent to the final rejection.

The subject matter on appeal is directed to a method for "fully" testing and burning-in integrated circuit chips before they are incorporated into a high density interconnect circuit or other hybrid circuit. This subject matter is adequately illustrated in independent claims 11 and 13, which are reproduced below:

11. A method for fully testing and burning-in integrated circuit chips before incorporating said chips into a high density interconnect circuit or other hybrid circuit, said chips having a plurality of chip pads thereon, said method comprising the steps of:

temporarily situating an integrated circuit chip on a test substrate with said chip pads facing away from said substrate, said test substrate having a plurality of pins extending through an entire thickness of said substrate but not in a region where said chip is situated, each of said chip pads being integrally connected to a temporary buffer pad, respectively, so as to provide an electrically conductive path therebetween;

temporarily electrically connecting said chip pads with predetermined ones of said pins at locations where said predetermined pins emerge from said test substrate by providing wires to electrically connect said predetermined pins to said temporary buffer pads, each of said wires being bonded at a first end to a respective one of said predetermined pins and being bonded at a second end to a respective one of said temporary buffer pads;

testing and burning-in said integrated circuit chip; and

retrieving said integrated circuit chip from said test substrate for subsequent incorporation into a high density interconnect circuit or other hybrid circuit unless said chip is not fully operative.

13. A method for fully testing and burning-in integrated circuit chips before incorporating said chips into a high density interconnect circuit or other hybrid circuit, said chips having a plurality of chip pads thereon and being coated with an insulative layer, each of said chip pads being electrically
connected to a temporary buffer pad, respectively, through a metal-filled via, respectively, said method comprising the steps of:

temporarily situating an integrated circuit chip on a test substrate with said chip pads facing away from said substrate, said test substrate having a plurality of pins extending through an entire thickness of said substrate but not in a region where said chip is situated;

temporarily electrically connecting said chip pads with predetermined ones of said pins at locations where said predetermined pins emerge from said test substrate by providing wires to electrically connect said predetermined pins to said temporary buffer pads, each of said wires being bonded at a first end to a respective one of said predetermined pins and being bonded at a second end to a respective one of said temporary buffer pads, each of said temporary buffer pads, respectively, being offset relative to each of said chip pads, respectively, connected thereto through a respective metal-filled via;

testing and burning-in said integrated circuit chip: and

retrieving said integrated circuit chip from said test substrate for subsequent incorporation into a high density interconnect circuit or other hybrid circuit unless said chip is not fully operative.

As evidence of obviousness, the examiner relies on the

following prior art:

Eichelberger et al. (Eichelberger '122)	4,884,122 (filed Aug. 05, 1988)	Nov. 28, 1989
Jones, II et al. (Jones)	4,861,944 (filed Dec. 09, 1987)	Aug. 29, 1989

Eichelberger et al. (Eichelberger '695) 4,783,695 Nov. 08, 1988
(filed Sep. 26, 1986)
Chihara et al. (Chihara) 4,745,018 May 17, 1988
(filed Sep. 08, 1987)
Werth 0 233 755 Aug. 26, 1987
(Published European Patent Application)

Bry et al., (Bry) IBM Technical Disclosure Bulletin,"Reusable Chip Test Package," Vol. 22, No. 4, pp. 1476 and 1477, (September 1979)(hereinafter referred to as "Bry").

Appellants' admitted prior art as seen from the specification at page 2, line 24 to page 3, line 5; page 4, line 15 to page 5, line 12; page 10, lines 14 to 17; page 15, lines 25-29; and page 16, lines 7 to 16 (hereinafter referred to as "appellants' admitted prior art").

The appealed claims stand rejected under 35 U.S.C. § 103 as follows:

(1) Claims 2, 4 and 11 through 13 as unpatentable over Bry in combination with Eichelberger '122 further taken with either Jones or appellants' admitted prior art;

(2) Claim 3 as unpatentable over Bry in combination with Eichelberger '122 further taken with either Jones or appellants' admitted prior art as applied to claims 2, 4 and 11 through 13 above, and further in view of either Chihara or Werth; and

(3) Claims 4 through 6 as unpatentable over Bry in combination with Eichelberger ‘122 further taken with either

Jones or appellants' admitted prior art as applied to claims 2,
4 and 11 through 13 above, and further in view of Eichelberger '695.

Having carefully considered all of the arguments advanced by appellants and the examiner in support of their respective positions, it is our conclusion that the above-noted rejections are not sustainable for essentially those reasons set forth at pages 17- 22 of the Brief and pages 4-7 of the Reply Brief. Absent the appellants' own disclosure, we can think of no reason why one of ordinary skill in this art would have been motivated to combine the diverse teachings of Bry, Eichelberger '122, Jones, Eichelberger '695, Chihara, Werth and appellants' admitted prior art as the examiner has proposed. As indicated by appellants, we find no suggestion or motivation to modify the testing device employed in the testing method of Bry to arrive at the claimed method inasmuch as Bry, Eichelberger '122 and Jones, for example, are directed to materially different testing methods which employ completely disparate types of testing devices (different structures) to promote different purposes. It is well settled

that it is the teachings of the prior art taken as a whole which must provide the motivation or suggestion to combine the prior art references. See Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988) and Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1143, 227 USPQ 543, 550-51 (Fed. Cir. 1985). The examiner cannot pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference would have fairly suggested to one of ordinary skill in the art. See Bausch & Lomb, Inc., v. Barnes-Hind/Hydrocurve Inc., 796 F.2d 443, 448, 230 USPQ 416, 419 (Fed. Cir. 1986), cert. denied, 484 U.S. 823 (1987); In re Kamm, 452 F.2d 1052, 1057, 172 USPQ 298, 301-02 (CCPA 1972). As the court in Uniroyal, 837 F.2d at 1051, 5 USPQ2d at 1438 stated "it is impermissible to use the claims as a frame and the prior art references as a mosaic to piece together a facsimile of the claimed invention." Accordingly, we conclude

that the examiner has not met his burden of presenting a prima facie case of obviousness.[2] See In re Rijckaert, 9 F.3d 1531,

[2] Having concluded that the examiner has not established a prima facie case of obviousness, we will not assess the sufficiency of the Rule 131 declarations of record referred to by appellants. However, we observe that these Rule 131 declarations have not been executed by all of the listed inventors in this application. See M.P.E.P. § 715.04 (Rev. 3, July 1997); 37 CFR § 1.131(a)(1).

1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993); In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

In view of the foregoing, we reverse the examiner's decision rejecting claims 2 through 6 and 11 through 13 under 35 U.S.C. § 103.

REVERSED

EDWARD C. KIMLIN Administrative Patent Judge	)	
BRADLEY R. GARRIS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
CHUNG K. PAK Administrative Patent Judge	)	

Appeal No. 93-1883
Application No. 07/759,691

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JENINE GILLIS

Appeal No. 93-1883
Serial No.
07/759,691

Judge PAK

Judge KIMLIN

Judge GARRIS

Received: 26 Aug 98

Typed: 27 Aug 98

DECISION: REVERSED

Send Reference(s): Yes No
or Translation(s)

Panel Change: Yes No

3-Person Conf. Yes No

Remanded: Yes No

Brief or Heard

Group Art Unit: 131

Index Sheet-2901 Rejection(s): _____

Acts 2: ____

Palm: ____

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Updated Monthly Report: ___